UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,746	06/26/2003	Jcom-Jin Chang	1572.1150	3810

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BERGER, AUBREY H

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _26 June 2003_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-14_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-14_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☒ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _6/26/03, 10/13/04_.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-14 are pending.

Priority

2.   Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which

papers have been placed of record in the file.

Information Disclosure Statement

3.   The information disclosure statement (IDS) submitted on 6/26/03 and 10/13/04 is

being considered by the examiner.

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

5.   Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite

for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention.

6.   Regarding claim 14, "wherein a security maintenance structure of the BIOS ROM

is not changed", is unclear.

Claim Rejections - 35 USC § 103

7.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

8.   Claims 1, 5-7, 11 and 13 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Challener et al., USPN 6,748,544 and further in view of Lin, USPN

6,892,323.

Regarding claim 1, Lin discloses a method of improving BIOS (Basic Input Output

System) security of a computer system (col.1, lines 13-17) and storing a check sum

value (col. 6, lines 20-23). Lin lacks or does not expressly disclose byte-adding a user

password and a product serial number. However, Challener discloses byte-adding a

user password and a product serial number (col. 8, lines 33-37 & col. 6, lines 13-17 and

fig. 5, #607). It would have been obvious to one of ordinary skill in the art at the time

the invention was made to modify the device of Lin with the device of Challener to store

a checksum value calculated by adding a user password and serial number in order to

secure and strengthen the password in the BIOS using a serial number as derived

secret as taught by Challener, (col. 8, lines 35-37). Lin further discloses comparing the

stored check sum value with a check sum value calculated by byte-adding an inputted

password and the product serial number of the BIOS ROM (col. 6, lines 20-23); and

enabling writing to the BIOS ROM when the stored check sum value and the calculated

check sum value are equal (col. 6, lines 22-28 and fig. 3, #206).

Regarding claim 5, Lin further discloses comprising: setting up a memory-mapped input/output region assigned as a BIOS writing protection region of a chipset having a GPIO (General Purpose Input Output) function as an input/output trap region and enabling an input/output trap (col. 2, lines 17- 26); allowing an event disabling a BIOS writing protection during operation of the computer system to occur (fig. 3, #202); setting up the input/output trap as disabled (col. 6, lines 5-20); determining the product serial number (Challener, col. 6, lines 13-17) of the BIOS ROM (col. 6, lines 20-23); allowing a user to input the inputted password when the product serial number is not a default value in manufacturing and calculating a check sum value by byte-adding the inputted password and the product serial number (Challener col. 8, lines 33-37 & col. 6, lines 13-17 and fig. 5, #607).

Regarding claim 6, Lin further discloses comprising: enabling the input/output trap after enabling writing to the BIOS ROM (fig. 3, #202 and #206).

Regarding claims 7 and 11, Lin lacks or does not expressly disclose displaying an error message. However, Challener discloses displaying an error message when the product serial number is a default value in manufacturing, or when the check sum values (Lin, col. 6, lines 20-23) are not equal (fig. 4, #517). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin

with the device of Challener to display an error message when the checksums do not match in order to notify the user the access in invalid, as taught by Challener (fig. 4, #517).

Regarding claim 13, Lin discloses a machine-readable medium that provides instructions, which, when executed by a machine, cause the machine to perform operations of improving BIOS (Basic Input Output System) security of a computer system (col.1, lines-13-17). Lin lacks or does not expressly disclose byte-adding a user password and a product serial number. However, Challener discloses byte-adding a user password and a product serial number (col. 8, lines 33-37 & col. 6, lines 13-17 and fig. 5, #607). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Challener to store a checksum value calculated by adding a user password and serial number in order to secure and strengthen the password in the BIOS using a serial number as derived secret as taught by Challener, (col. 8, lines 35-37). Lin further discloses comparing the stored check sum value with a check sum value calculated by byte-adding an inputted password and the product serial number of the BIOS ROM (col. 6, lines 20-23); and enabling writing to the BIOS ROM when the stored check sum value and the calculated check sum value are equal (col. 6, lines 22-28 and fig. 3, #206).

9.   Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in

view of Challener as applied to claim 1 above, and further in view of Cromer et al, US

Patent Application Publication 2002/0120845.

Regarding claim 2, Lin in view of Challener discloses the method of improving BIOS

security according to claim 1. Lin lacks or does not expressly disclose determining if the

user password is set up on a POST. However, Cromer discloses wherein the storing

the check sum value comprises: determining if the user password is set up on a POST

(Power On Self Test) (¶[0020-0021]). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to modify the device of Lin in view of

Challener with the device of Cromer to determine of the password is set up in POST in

order to authenticate the requester of the BIOS update by retrieving the current

administrator password as taught by Cromer (¶[0021]). Lin further discloses

determining the product serial number (Challener, col. 6, lines 16-17), of the BIOS ROM

(col. 5, lines 55-57), in a case that the user password is set up (Challener, fig. 4, #503);

and storing an added check sum value that is calculated by byte-adding the user

password and the product serial number in a memory when the product serial number is

not a default value in manufacturing (col. 8, lines 33-37 & col. 6, lines 13-17 and fig. 5,

#607).

Regarding claim 3, Lin further discloses comprising: setting up a memory-mapped

input/output region assigned as a BIOS writing protection region of a chipset having a

GPIO (General Purpose Input Output) function as an input/output trap region and enabling an input/output trap (col. 2, lines 18-27).

Regarding claim 4, Lin lacks or does not expressly disclose storing the checksum in RAM or NVRAM. However, Challener further discloses wherein the storing the added check sum value (Lin, col. 6, line 20-23) in the memory comprises: storing the added check sum value in a CMOS RAM or a PNP NVRAM (col. 6, lines 12-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lin with the device of Challener to store the checksum in NVRAM in order to retain the stored checksum, as taught by Challener (col. 6, lines 12-15).

10.   Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Challener as applied to claim 5 above, and further in view of Freeman et al., US Publication No. 2004/003265.

Regarding claims 8-10, Lin further discloses wherein the allowing of the event disabling of the BIOS writing protection to occur comprises allowing the input/output trap to occur (fig. 3, #202 and #206). Lin lacks or does not expressly disclose allowing writing to the BIOS ROM by a PNP NVRAM (Plug And Play Non-Volatile Random Access Memory) manager to occur. However, Freeman discloses allowing writing to the BIOS ROM by a PNP NVRAM (Plug And Play Non-Volatile Random Access Memory) manager to occur (¶[0009]). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the device of Lin with the device of Freeman to utilize a

PNP NVRAM in order to write to the BIO ROM as taught by Freeman (¶[0009]).

Regarding claim 12 Lin lacks or does not expressly disclose displaying an error

message. However Challener discloses displaying an error message when the product

serial number is a default value in manufacturing, or when the check sum values (Lin,

col. 6, lines 20-23) are not equal (fig. 4, #517). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify the device of Lin

with the device of Challener to display an error message when the checksums do not

match in order to notify the user the access in invalid, as taught by Challener (fig. 4,

#517).

Claim Rejections - 35 USC § 102

11.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12.   Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Freeman.

Regarding claim 14, Freeman discloses method of improving BIOS (Basic Input Output System) security of a computer system (abstract), comprising: receiving an inputted password (fig. 2, #203); and enabling writing to a BIOS ROM based upon the inputted password (fig. 2, #204 and #210), wherein a security maintenance structure of the BIOS ROM is not changed (fig. 2, #209).
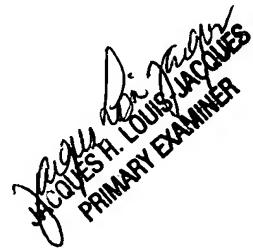
Conclusion

13.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aubrey H. Berger whose telephone number is (571)272-8155. The examiner can normally be reached on Monday - Thursday, and alternate Friday's.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571)272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AHB